REMARKS

In the Office Action, Claims 1-29 were examined. Claims 1-4 and 6-9 stand rejected, Claims 5 and 10 are objected and Claims 11-29 are allowed. In response to the Office Action, no claims are amended, no claims are cancelled and no claims are added. Applicants respectfully request reconsideration of pending Claims 1-29 in view of the following remarks.

I. Claims Rejected Under 35 U.S.C. §102

The Examiner rejects Claims 1-4 and 6-8 under 35 U.S.C. §102(e) as being unpatentable over U.S. Patent No. 6,477,177 issued to Potts ("Potts"). Applicants respectfully traverse this rejection.

Regarding Claims 1 and 6, Claims 1 and 6 recite the following claim features, which are neither disclosed nor suggested by Potts:

> enabling a hardware accelerator selected from a plurality of hardware accelerators according to at least one bit of a register within the register file set by a processing element; and
>
> granting the processing element ownership over the selected hardware accelerator. (Emphasis added.)

As indicated by the Examiner's rejection of Claims 1 and 6, the Examiner equates the plurality of processing elements, as recited by Claims 1 and 6, to processor #1 and processor #2, as disclosed by Potts. (*See*, pg. 2, ¶5 of Office Action mailed August 10, 2005.) Assuming, arguendo, that processor #1 and processor #2, as taught by Potts, disclose the plurality of processing elements, as recited by Claims 1 and 6, Potts is devoid of, and hence, fails to provide any disclosure, teaching or suggestion regarding the enabling of a hardware accelerator selected from a plurality of hardware accelerators by setting a bit within a register file by a processor element, which desires ownership over the selected hardware accelerator, as recited by Claims 1 and 6.

In contrast to the above-recited features of Claims 1 and 6, Potts discloses:

> an improved digital interface for an AC '97 controller having expandable and automatic capabilities including effectively increased bus width, accessibility by a plurality of processors, and creation of tag bits. (col. 1, lines 14-18.) (Emphasis added.)

As further disclosed by Potts:

> Conventional AC '97 split-architecture systems accommodate only one processor, treating the AC '97 link as a single device to be used by only one processor. However, it has been appreciated by the present inventor that more recent applications would benefit from access to the AC '97 link and the AC '97 Analog sub-system by a plurality of processors, either all within the AC controller sub-system 500 and/or external to the AC controller sub-system 500. There is thus a need for an interface in an AC controller system which can provide access to the AC '97 link and AC '97 Analog sub-system by any of a plurality of processors. (col. 3, lines 1-11.) (Emphasis added.)

Applicants respect fully submit that the disclosure in Potts is limited to enabling an AC'97 split-architecture system to accommodate more than one processor. (*See*, supra.) Applicants respectfully submit that the inclusion of the capability within an AC '97 split-architecture system to accommodate more than one processor, such that the AC '97 link is not treated as a single device to be used by only one processor, provides no teachings nor suggestions regarding the capability to share a plurality of hardware accelerators among a plurality of processing elements of a media signal processor to enable a processing element to gain ownership over a selected hardware accelerator, as recited by Claims 1 and 6.

According to the Examiner, the features of Claims 1 and 6 are disclosed by Potts at col. 5, line 63 - col. 6, line 15. As recited by such passages:

> For example, if processor #1 desires to write to the command data register of the AC Analog via time slot 2 (602 in FIG. 6), processor #1 would set bit 2 in the configuration control register 220 (FIG. 2). Thereafter, processor #1 polls bit 0 of the configuration control register 220 until it goes high, then polls bit 2 of the configuration control register 220 until it goes high, indicating that access to the command data register is granted to processor #1 via the temporary register 212 of time slot 2. Thus, once bit 0 goes high, any bit that is set, i.e., any of bits 1 to 12, would indicate that the processor has been granted access to write to the corresponding time slot register.
>
> Preferably, bit 0 of the configuration control register 220 is cleared upon writes to the configuration control register 220.
>
> When a processor has completed its access to a particular resource, e.g., time slot register, and desires to release its ownership of that resource, the processor can clear the corresponding bit in the configuration control register 220 (i.e., write a zero to the bit location). (col. 5, line 63 - col. 6, line 15.) (Emphasis added.)

As further described by the above passage, Potts describes the functionality provided by such passage as follows:

> In accordance with the principles of the present invention, access is provided to an AC '97 link or other digital serial interface by any of a plurality of processing agents with an arbitration scheme which is provided on a per channel basis, either during power up of the AC '97 devices or as the accesses occur. Thus, e.g., each channel or time slot in an AC '97 link can be considered to be an independent resource which is configurable for access by any of a plurality of requesting processors. (col. 4, lines 49-58.) (Emphasis added.)

As mandated by case law, Applicants respectfully assert that the Patent Office has failed to adequately set forth a *prima facie* rejection under 35 U.S.C. §102(e). "Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*" *Lindemann Maschinenfabrik v. American Hoist & Derrick* ("Lindemann"), *730 F.2d 452, 1458 (Fed. Cir. 1994)*(emphasis added). Additionally, each and every element of the claim must be exactly disclosed in the anticipatory reference. *Titanium Metals Corp. of American v. Banner* ("Banner Titanium"), *778 F.2d 775, 777 (Fed. Cir. 1985).*

Here, the disclosure in Potts is limited to enabling multiple processors with an arbitration scheme, which is provided on a per-channel basis of an AC '97 device. (*See*, col. 4, lines 49-58.) As indicated by Potts, each channel or time slot in the AC link can be considered as an independent resource, which is configurable for access by any of a plurality of requesting processors. (*See*, col. 4, lines 55-58.) Applicants respectfully submit that the capability to provide each channel, or time slot, within an AC '97 link as an independent resource inevitably results in the sharing of the AC '97 link between each of the processors, as disclosed in Potts. (*See*, supra.)

Conversely, as recited by Claims 1 ad 6, a hardware accelerator selected from a plurality of hardware accelerators is enabled based on at least one bit of a register, which is set by a processing element, to enable the processing element to gain ownership over the selected hardware accelerator. Applicants respectfully submit that gaining access to a channel, or time slot, of an AC link fails to disclose or suggest the providing of ownership to a processing element over a selected hardware accelerator by setting a bit associated with the hardware accelerator, as recited by Claims 1 and 6.

Hence, Applicants respectfully submit that the arbitration scheme to enable each channel, or time slot, in an AC link to be considered as an independent resource, as disclosed by Potts, fails to exactly disclose the enabling of a hardware accelerator, which is selected from a plurality of hardware accelerators according to at least one bit of a register file that is set by a processing element to enable the processing element to gain ownership over the selected hardware accelerator, as recited by Claims 1 and 6.

Accordingly, Applicants respectfully submit that the Examiner is prohibit from relying on Potts as an anticipatory reference, since Potts fails to exactly disclose each and every element of Claims 1 and 6. Banner Titanium, supra. Accordingly, Applicants respectfully submit that the Examiner fails to set forth a *prima facie* case of anticipation, since the Examiner fails to illustrate the presence in a single prior art reference disclosure of Potts regarding each and every element recited by Claims 1 and 6, as arranged in the respective claims. Lindemann, supra.

Consequently, Applicants respectfully submit that Claims 1 and 6 are patentable over Potts, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(e) rejection of Claims 1 and 6.

Regarding 2-4, Claims 2-4, based on their dependency from Claim 1, are also patentable over Potts, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(e) rejection of Claims 2-4.

Regarding 7-9, Claims 7-9 based on their dependency from Claim 6, are also patentable over Potts, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(e) rejection of Claims 7-9.

V. Allowable Subject Matter

Applicants note with appreciation the Examiner's indication that Claims 11-27 are allowed. Regarding the allowance of Claims 11-27, Applicants would respectfully like to thank the Examiner for recognizing the allowability of such claims.

The Examiner has indicated that Claims 5 and 10 would be allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims.

Regarding Claims 5 and 10, Applicants would respectfully like to thank the Examiner for recognizing the allowability of Claims 5 and 10 if incorporated into their respective independent Claims 1 and 6. However, Applicants respectfully submit that Claims 5 and 10 are also patentable, based on their dependency from Claims 1 and 6, respectfully. Therefore, Applicants respectfully request that the Examiner allow Claims 5 and 10.

CONCLUSION

In view of the foregoing, it is submitted that Claims 1-29 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: October 13 2005

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CERTIFICATE OF MAILING:
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on October 13, 2005

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Marilyn Bass October 13, 2005